

Code No: 133AJ

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

- 1.a) What are 2's complement and 9's complement of a numbers? Give examples. [2]
- b) State and prove De Morgan theorems. [3]
- c) What are minterms and maxterms? Give examples for each. [2]
- d) Define pair quad and octet in K-Maps and give examples. [3]
- e) Draw the logic circuit of a full adder and give its truth table. [2]
- f) Write the functions of a decoder and multiplexer. [3]
- g) Draw the logic diagram of a master slave J-K flip-flop. [2]
- h) Describe the race free state assignment in asynchronous sequential circuits. [3]
- i) What are PLAs and PALs? [2]
- j) Explain about arithmetic operations with examples. [3]

PART-B

(50 Marks)

- 2.a) Explain various number systems and codes and their conversion with examples for each.
- b) Simplify the following Boolean expressions to a minimum number of literals
(i) $ABC + A'B + ABC'$ (ii) $xy + x(wz + wz')$ [5+5]

OR

- 3.a) Express the following numbers in decimal : $(10110.0101)_2$, $(16.5)_{16}$, $(26.24)_8$.
- b) Demonstrate by means of truth tables the Boolean Associative law and distributive law.
- c) Simplify the Boolean expression to minimum number of literals: $(A+B)(A'+B')$. [10]
- 4.a) Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates
 $F(A,B,C,D) = \sum(0,2,4,5,6,7,8,10,13,15)$
- b) Show that the dual of the exclusive OR is also its complement. [5+5]

OR

- 5.a) Draw the multiple level NAND circuit for the following expression:
 $(AB' + CD')E + BC(A+B)$
- b) Simplify the following four variable Boolean function and implement the same using NAND logic. $F(A,B,C,D) = \sum(0,2,4,5,6,7,8,10,13,15)$ [5+5]

- 6.a) Construct a 4-bit BCD adder-subtractor circuit using BCD adder and 9's complementer.
b) Explain the working and functions of decoders and encoders. Construct 2/4 line decoder with logic gates with enable input. [5+5]

- OR
7.a) Construct a 4 bit 2's complement adder using full adders and perform addition and subtraction by taking 4-bit numbers with examples.
b) Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates. [5+5]

- 8.a) Design 4-bit shift register using D flip-flops and explain its working with the help of timing diagrams.

- b) Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6, use JK flip-flops. [5+5]

OR

- 9.a) Draw the circuit diagram of a 4-bit binary counter with parallel load and explain its working with its function table.

- b) Design a 4 bit synchronous counter with D flip - flops and explain its working. [5+5]

- 10.a) Given 32×8 ROM with enable input. Show the external connections necessary to construct a 128×8 ROM with 4 chips and a decoder.

- b) Explain the working of a PLA with a schematic and implement the following two Boolean functions with a PLA:

$$F_1(A, B, C) = \sum(0, 1, 2, 4) \text{ and } F_2(A, B, C) = \sum(0, 5, 6, 7). \quad [5+5]$$

OR

- 11.a) Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:

$$F_1(A, B, C) = \sum(0, 1, 3, 5) \text{ and } F_2(A, B, C) = \sum(1, 2, 4, 7)$$

- b) What are sequential programmable devices? Draw the sequential programmable logic for a basic microcell logic. [5+5]

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R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

SIGNALS AND STOCHASTIC PROCESS

(Common to ECE, ETM)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 Marks)

- 1.a) Give the condition for the physical reliability of a system. [2]
- b) What are the properties of convolution? [3]
- c) State any two properties of Fourier series. [2]
- d) Find the Fourier transform of the signal $x(t) = 20 \text{ sinc}(20t)$. [3]
- e) Explain the concept of region of convergence for Laplace transforms. [2]
- f) Write the differentiation in time property of Laplace transform. [3]
- g) Define random process. [2]
- h) Give the relation between correlation and Convolution. [3]
- i) Verify that the cross spectral density of two uncorrelated stationary random processes is an impulse function. [2]
- j) Define cross -spectral density and its examples. [3]

PART-B

(50 Marks)

2. Graphically convolve the signals

$$X_1(t) = \begin{cases} 1; & \text{for } -T \leq t \leq T \\ 0; & \text{elsewhere} \end{cases} \quad \text{and} \quad X_2(t) = \begin{cases} 1; & \text{for } -2T \leq t \leq 2T \\ 0; & \text{elsewhere} \end{cases} \quad [10]$$

OR

- 3.a) What is an LTI system? Explain the properties of it. [5+5]
- b) Find whether $x(t) = A e^{-\alpha(t)} u(t)$, $\alpha > 0$ is an energy signal or not.

- 4.a) Obtain the Fourier series coefficients for $x(t) = A \sin \omega_0 t$. [5+5]
- b) What is the Significance of Hilbert Transform? Explain.

OR

5. Define Fourier transform. Explain the properties of Fourier transform. [10]

- 6.a) Find the Laplace transform of $x(t) = -t^2 e^{-at} u(-t)$ and indicate its ROC. [5+5]
- b) Find the inverse Laplace transform of $x(s) = 5(s+5)/s(s+3)(s+7)$; $\text{Re}(s) > -3$.

OR

- 7.a) Find the inverse Z- transform of $X(z) = \frac{1+3z^{-1}}{1+3z^{-1}+2z^{-2}}$ for different possible ROCs.

- b) Give the relationship between z-transform and Laplace Transform. [7+3]

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- 8.a) A Random Process $X(t) = A \cos(2\pi f_c t)$, where A is a Gaussian Random Variable with zero mean and unity variance, is applied to an ideal integrator, that integrates with respect to 't', over $(0, t)$. Check the output of integrator for stationarity.

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- b) A random Process is defined as $X(t) = 3 \cos(2\pi t + Y)$, where Y is a random Variable with $p(Y=0) = p(Y=\pi) = 1/2$. Find the mean and Variance of the Random Variable $X(2)$. [5+5]

OR

- 9.a) State and prove properties of cross correlation function.

- b) If the PSD of $X(t)$ is $S_{xx}(\omega)$. Find the PSD of $dx(t)/dt$. [5+5]

- 10.a) Find and plot the Autocorrelation function of

(i) Wide band White noise (ii) Band-Pass White noise.

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- b) Derive the expression for the Cross Spectral Density of the input Process $X(t)$ and the output process $Y(t)$ of an LTI system in terms of its Transfer function. [5+5]

OR

11. The auto correlation function of a random process $X(t)$ is $R_{XX}(\tau) = 3 + 2 \exp(-4\tau^2)$

a) Evaluate the power spectrum and average power of $X(t)$.

- b) Calculate the power in the frequency band $-1/\sqrt{2} < \omega < 1/\sqrt{2}$. [5+5]

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R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

ENVIRONMENTAL STUDIES

(Common to ME, MIE)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

- 1.a) Define the term Ecology.
- b) Define food chains and food webs.
- c) Define living and non living resources.
- d) Explain what is water logging?
- e) Define "Biodiversity".
- f) Explain the phenomenon of Biodiversity of India.
- g) Define term "Environment Pollution".
- h) What is "Air Pollution"?
- i) Describe biomedical waste management.
- j) Describe Risk Assessment.

[2]
[3]
[2]
[3]
[2]
[3]
[2]
[3]
[2]
[3]

PART- B

(50 Marks)

- 2.a) Explain the concept of Ecosystem and its components.
- b) What are ecological pyramids?
- c) Explain different kinds of pyramids.

[3+3+4]

OR

- 3.a) Describe the structure and functions of an Ecosystem.
- b) Explain the energy flow in the ecosystem.
- c) Explain about the Forest Ecosystem and its functions.

[3+3+4]

- 4.a) Define the term "Resources" and Natural Resources. Classify the Worlds Natural resources.

- b) Describe the Forest Resources and Dangers of Deforestation.
- c) What are the Benefits and Problems concerned with dams?

[4+3+3]

OR

- 5.a) Describe the water resources available in Nature.
- b) What are the advantages and disadvantages of construction of dams across rivers?
- c) Describe the water resources of the environment, and what do you mean by water cycle.

[3+3+4]

- 6.a) Give the salient features of National Biodiversity act.
- b) What are threats to Biodiversity? How do you protect Biodiversity from them?
- c) Explain why India is called a mega Diversity Nation?

[3+3+4]

OR

- 7.a) Explain the Value of Biodiversity.
b) Describe the phenomenon of ecosystem management.
c) Write notes on "Hot spots of Biodiversity". [3+4+3]

- 8.a) Explain the different kinds of "Environmental Pollution".
b) Explain the sources of Atmospheric pollution along with its Control measures.
c) What is the effect of Carbon monoxide on Environment? [4+3+3]

OR

- 9.a) Explain about impact of water pollution.
b) Explain about solid waste management. [5+5]

- 10.a) Briefly explain the Wild Life Protection Act.
b) Write a note on Water Pollution prevention and control Act.
c) Explain the Air Pollution prevention and control Act. [4+3+3]

OR

- 11.a) Explain the Hazardous waste management.
b) Explain the Municipal Solid waste management and its handling rules.
c) Write short notes on Environmental Impact Assessment. [4+3+3]

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Code No: 123BU

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

- 1.a) $AB + A'C + BC = AB + A'C$ represents which theorem? [2]
- b) Find the radix of the number system, if $302/20 = 12.1$. [3]
- c) How many adjacent cells are there to each cell in a n variable K-map? [2]
- d) What are wired logic? [3]
- e) Compare latch and flip flop. [2]
- f) What are timing considerations? [3]
- g) List out the drawbacks of ripple counters? [2]
- h) Draw the state diagram for SR-FF. [3]
- i) What are capabilities of finite state machine? [2]
- j) Mention the salient features of ASM chart. [3]

PART-B

(50 Marks)

- 2.a) Write the properties of XOR gates. [5+5]
 - b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal. [5+5]
- OR**
- 3.a) Simplify the following Boolean expressions using the Boolean theorems.
(i) $(A+B+C)(B'+C) + (A+D)(A'+C)$ (ii) $(A+B)(A+B')(A'+B)$
 - b) Why a NAND and NOR gates are known as universal gates? Simulate all the Gates. [5+5]
- 4.a) Minimize the following expressions using K-map and realize using NAND Gates.
 $f = \sum m(1,3,5,8,9,11,15) + d(2,13)$
 - b) Minimize the following expression using K-map and realize using NOR Gates.
 $f = \prod M(1,2,3,8,9,10,11,15) \cdot d(7,1,5)$ [5+5]
- OR**
- 5.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
 - b) Realize the function $f(A,B,C,D) = \prod[(1,4,6,10,14) + d(0,8,11,15)]$ using
(i) 16:1 MUX (ii) 8:1 MUX. [5+5]

- 6.a) Explain the operation of R-S master slave flip flop. Explain its truth table.
b) Explain about the realization of SR flip-flop, JK flip-flop using D flip-flop. [5+5]

OR

- 7.a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.
b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits. [5+5]

- 8.a) Design, draw and explain a synchronous MOD-12 down-counter using J-K flip-flop.

- b) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams. [5+5]

OR

- 9.a) Explain the differences between asynchronous and synchronous counters. Design a MOD-10 ripple counter.

- b) Design and construct MOD-5 synchronous counter using JK flip flops. [5+5]

- 10.a) Compare Mealy and Moore machines.

- b) Explain the procedure for state minimization using merger graph and merger table with example. [5+5]

OR

- 11.a) Differentiate between an ASM chart and a conventional flow chart.

- b) Explain in detail the ASM technique of designing a sequential circuit. [5+5]

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Code No: 123CT

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

- 1.a) What is Diminished Radix Complement? [2]
- b) What is Minterms and Maxterms? [3]
- c) What is Prime Implicants? [2]
- d) What is don't-care conditions? Explain it uses. [3]
- e) Explain about 4-bit Binary Adder. [2]
- f) Explain about Multiplexers with three-state gates. [3]
- g) Explain about characteristic equation for jk flip flop. [2]
- h) Define the following terms of a flip flop.
i) Hold time ii) Set up time iii) Propagation delay time. [3]
- i) Explain about sequential memory. [2]
- j) Explain about the memory read and write operations. [3]

PART-B

(50 Marks)

- 2.a) If the numbers $(+9,742)_{10}$ and $(+641)_{10}$ are in signed magnitude format, their sum is $(+10,383)_{10}$ and requires five digits and a sign. Convert the numbers to signed-10's complement form and find the following sums:
(i) $(+9,742) + (+641)$ (ii) $(+9,742) + (-641)$
- b) Convert the hexadecimal number 64CD H to binary and then convert it from binary to octal. [5+5]

OR

- 3.a) Express the complement of the following function F in sum of minterms form
 $F(A,B,C,D) = \sum(2, 4, 7, 10, 12, 14)$
- b) Show that the dual of the exclusive OR is equal to its complement. [5+5]
- 4.a) Simplify the following Boolean expressions, using four-variable maps:
i) $A'B'C'D' + AC'D + B'CD' + A'BCD + BC'D$
ii) $A'B'C'D' + BC'D + A'C'D + A'BCD + ACD'$
- b) Find all the prime implicants for the following Boolean functions, and determine which are essential: $F(w, x, y, z) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ [5+5]

OR

- 5.a) Draw a NAND logic diagram that implements the complement of the following function:
 $F(A,B,C,D) = \sum(0, 1, 2, 3, 6, 10, 11, 14)$
- b) Find the minterms of the following Boolean expressions by first plotting each function in a map:
(i) $xy + yz + xy'z$ (ii) $C'D + ABC' + ABD' + A'B'D$ [5+5]

6. Design a combinational circuit with three inputs, x, y and z and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. [10]

OR

- 7.a) Implement a full adder with two 4×1 multiplexers.
b) Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority. [5+5]

- 8.a) Draw the logic diagram of a four-bit binary-ripple countdown counter using flip-flops that trigger on the positive edge of the clock.
b) Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain. [5+5]

OR

- 9.a) Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.
b) Compare merits and demerits of ripple and synchronous counters. [5+5]

10. A $16K \times 4$ memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.
a) What is the size of each decoder, and how many AND gates are required for decoding the address?
b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000. [10]

OR

- 11.a) Explain about different types of ROM.
b) Explain about Cache memory. [5+5]

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Code No: 113AF

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

ENVIRONMENTAL STUDIES

(Common to ME, AE, MIE)

Time: 3 Hours

Max. Marks: 75

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PART- A

(25 Marks)

- 1.a) Define the term Ecology.
- b) Define food chains and food webs.
- c) Define living and non living resources.
- d) Explain what is water logging?
- e) Define "Biodiversity".
- f) Explain the phenomenon of Biodiversity of India.
- g) Define term "Environment Pollution".
- h) What is "Air Pollution"?
- i) Describe biomedical waste management.
- j) Describe Risk Assessment.

[2]
[3]
[2]
[3]
[2]
[3]
[2]
[3]
[2]
[3]

PART- B

(50 Marks)

- 2.a) Explain the concept of Ecosystem and its components.
- b) What are ecological pyramids?
- c) Explain different kinds of pyramids.

[3+3+4]

OR

- 3.a) Describe the structure and functions of an Ecosystem.
- b) Explain the energy flow in the ecosystem.
- c) Explain about the Forest Ecosystem and its functions.
- 4.a) Define the term "Resources" and Natural Resources. Classify the Worlds Natural resources.
- b) Describe the Forest Resources and Dangers of Deforestation.
- c) What are the Benefits and Problems concerned with dams?

[3+3+4]

[4+3+3]

OR

- 5.a) Describe the water resources available in Nature.
- b) What are the advantages and disadvantages of construction of dams across rivers?
- c) Describe the water resources of the environment, and what do you mean by water cycle.
- 6.a) Give the salient features of National Biodiversity act.
- b) What are threats to Biodiversity? How do you protect Biodiversity from them?
- c) Explain why India is called a mega Diversity Nation?

[3+3+4]

[3+3+4]

OR

- 26 26 26 26 26 26 26 26
- 7.a) Explain the Value of Biodiversity.
b) Describe the phenomenon of ecosystem management.
c) Write notes on "Hot spots of Biodiversity".

[3+4+3]

- 26 26 26 26 26 26 26 26
- 8.a) Explain the different kinds of "Environmental Pollution".
b) Explain the sources of Atmospheric pollution along with its Control measures.
c) What is the effect of Carbon monoxide on Environment?

[4+3+3]

OR

- 9.a) Explain about impact of water pollution.
b) Explain about solid waste management.

[5+5]

- 26 26 26 26 26 26 26 26
- 10.a) Briefly explain the Wild-Life Protection Act.
b) Write a note on Water Pollution prevention and control Act.
c) Explain the Air Pollution prevention and control Act.

[4+3+3]

OR

- 11.a) Explain the Hazardous waste management.
b) Explain the Municipal Solid waste management and its handling rules.
c) Write short notes on Environmental Impact Assessment.

[4+3+3]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE)

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- c) How many adjacent cells are there to each cell in a n variable K-map? [2]
- d) What are wired logic? [3]
- e) Compare latch and flip flop. [2]
- f) What are timing considerations? [3]
- g) List out the drawbacks of ripple counters? [2]
- h) Draw the state diagram for SR-FF. [3]
- i) What are capabilities of finite state machine? [2]
- j) Mention the salient features of ASM chart. [3]

PART-B

(50 Marks)

- 2.a) Write the properties of XOR gates. [5+5]
 - b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal. [5+5]
- OR**
- 3.a) Simplify the following Boolean expressions using the Boolean theorems.
(i) $(A+B+C)(B'+C) + (A+D)(A'+C)$ (ii) $(A+B)(A+B')(A'+B)$
 - b) Why a NAND and NOR gates are known as universal gates? Simulate all the Gates. [5+5]
- 4.a) Minimize the following expressions using K-map and realize using NAND Gates.
 $f = \sum m(1,3,5,8,9,11,15) + d(2,13)$
 - b) Minimize the following expression using K-map and realize using NOR Gates.
 $f = \prod M(1,2,3,8,9,10,11,15) \cdot d(7,1,5)$ [5+5]
- OR**
- 5.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
 - b) Realize the function $f(A,B,C,D) = \prod(1,4,6,10,14) + d(0,8,11,15)$ using
(i) 16:1 MUX (ii) 8:1 MUX. [5+5]

- 6.a) Explain the operation of R-S master slave flip flop. Explain its truth table.
b) Explain about the realization of SR flip-flop, JK flip-flop using D flip-flop. [5+5]

OR

- 7.a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.
b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits. [5+5]

- 8.a) Design, draw and explain a synchronous MOD-12 down-counter using J-K flip-flop.

- b) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams. [5+5]

OR

- 9.a) Explain the differences between asynchronous and synchronous counters. Design a MOD-10 ripple counter.

- b) Design and construct MOD-5 synchronous counter using JK flip flops. [5+5]

- 10.a) Compare Mealy and Moore machines.

- b) Explain the procedure for state minimization using merger graph and merger table with example. [5+5]

OR

- 11.a) Differentiate between an ASM chart and a conventional flow chart.

- b) Explain in detail the ASM technique of designing a sequential circuit. [5+5]

Code No: 113BS

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 Hours

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PART-A

(25 Marks)

- 1.a) What is Diminished Radix Complement? [2]
- b) What is Minterms and Maxterms? [3]
- c) What is Prime Implicants? [2]
- d) What is don't-care conditions? Explain it uses. [3]
- e) Explain about 4-bit Binary Adder. [2]
- f) Explain about Multiplexers with three-state gates. [3]
- g) Explain about characteristic equation for jk flip flop. [2]
- h) Define the following terms of a flip flop.
i) Hold time ii) Set up time iii) Propagation delay time. [3]
- i) Explain about sequential memory. [2]
- j) Explain about the memory read and write operations. [3]

PART-B

(50 Marks)

- 2.a) If the numbers $(+9,742)_{10}$ and $(+641)_{10}$ are in signed magnitude format, their sum is $(+10,383)_{10}$ and requires five digits and a sign. Convert the numbers to signed-10's complement form and find the following sums:
(i) $(+9,742) + (+641)$ (ii) $(+9,742) + (-641)$
- b) Convert the hexadecimal number 64CD H to binary and then convert it from binary to octal. [5+5]

OR

- 3.a) Express the complement of the following function F in sum of minterms form
 $F(A,B,C,D) = \sum(2, 4, 7, 10, 12, 14)$
- b) Show that the dual of the exclusive OR is equal to its complement. [5+5]
- 4.a) Simplify the following Boolean expressions, using four-variable maps:
i) $A'B'C'D' + AC'D + B'CD' + A'BCD + BC'D$
ii) $A'B'C'D' + BC'D + A'C'D + A'BCD + ACD'$
- b) Find all the prime implicants for the following Boolean functions, and determine which are essential: $F(w, x, y, z) = \sum(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ [5+5]

OR

- 5.a) Draw a NAND logic diagram that implements the complement of the following function:
 $F(A,B,C,D) = \sum(0, 1, 2, 3, 6, 10, 11, 14)$.
- b) Find the minterms of the following Boolean expressions by first plotting each function in a map:
(i) $xy + yz + xy'z$ (ii) $C'D + ABC' + ABD' + A'B'D$. [5+5]

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6. Design a combinational circuit with three inputs, x, y and z and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. [10]

OR

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- 7.a) Implement a full adder with two 4×1 multiplexers.
b) Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority. [5+5]

- 8.a) Draw the logic diagram of a four-bit binary-ripple countdown counter using flip-flops that trigger on the positive edge of the clock.
b) Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain. [5+5]

OR

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- 9.a) Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.
b) Compare merits and demerits of ripple and synchronous counters. [5+5]

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10. A $16K \times 4$ memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.
a) What is the size of each decoder, and how many AND gates are required for decoding the address?
b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000. [10]

OR

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- 11.a) Explain about different types of ROM.
b) Explain about Cache memory. [5+5]

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8.a) A Random Process $X(t) = A \cos(2\pi f_c t)$, where A is a Gaussian Random Variable with zero mean and unity variance, is applied to an ideal integrator, that integrates with respect to 't', over $(0, t)$. Check the output of integrator for stationarity.

26 b) A random Process is defined as $X(t) = 3 \cos(2\pi t + Y)$, where Y is a random Variable with $p(Y=0) = p(Y=\pi) = 1/2$. Find the mean and Variance of the Random Variable $X(2)$. [5+5]

OR

9.a) State and prove properties of cross correlation function.

b) If the PSD of $X(t)$ is $S_{xx}(\omega)$. Find the PSD of $dx(t)/dt$. [5+5]

10.a) Find and plot the Autocorrelation function of

(i) Wide band White noise (ii) Band Pass White noise.

26 b) Derive the expression for the Cross Spectral Density of the input Process $X(t)$ and the output process $Y(t)$ of an LTI system in terms of its Transfer function. [5+5]

OR

11. The auto correlation function of a random process $X(t)$ is $R_{XX}(\tau) = 3 + 2 \exp(-4\tau^2)$

a) Evaluate the power spectrum and average power of $X(t)$.

b) Calculate the power in the frequency band $-1/\sqrt{2} < \omega < 1/\sqrt{2}$. [5+5]

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